Efficiency of Synchronous and Asynchronous Buck-Converter at Low Output Current.

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Abstract

In this paper both synchronous and asynchronous buck-converter were designed to work in continuous conduction mode "CCM" and to deliver small load current. Then the two topologies were tested in terms of efficiency at small load current by use of different values of switching frequencies (range from 150 KHz to 1MHz) and three separated values of duty-cycle (0.4, 0.6 and 0.8).

Obtained results turns out that efficiency of both synchronous and asynchronous buck-converter "*switching step-down voltage regulator*" responds in a negative manner to the increase in the switching frequency. However, this impact is being stronger in synchronous topology because of magnifying effect of losses related to switching frequency compared to those related to conduction when working at small load currents; this behavior makes obtained efficiency of both topologies in convergent levels when they operated to deliver small output current especially when working with higher switching frequencies. Larger duty-cycle can rise up the efficiency of both topologies.

Keywords: - Buck-converter, Efficiency of buck-converter, Switching voltage regulators, Continuous conduction mode, Duty-cycle, and Switching and conduction losses in MOSFETs.

1- Introduction

In the last years, traditional power supplies were replaced by switching mode power supplies "SMPS" in most electronic and power applications especially in portable devices, computers, and telecommunications. This modern generation of power supplies made a big improvements on many performance indicators, mainly in power saving, efficiency gaining and size reduction. One of the public application of SMPS is buck-converter or what sometimes called "dc to dc step-down converter" in which a switch element "MOSFET" is controlled by pulse width modulated "PWM" control signal in order to regulate dc voltage across load "V_{out}" derived from higher dc input voltage "V_{in}", the value of load voltage depends on the ratio of ON-time duration "Ton" to the PMW time period "T". Because of small series ON- resistance "Rds_{on}" of the switch element during the short ON-time duration the power dissipated across the switch element is very small compared with the power dissipated across the series-pass element in the traditional step-down dc to dc converter, and that is the major technique in the modern dc to dc converter which led to increased efficiency and comprises the size of needed heat-sink and most of the other improvements in the performance. Surely, a new problem had appeared because of using the PWM technique like electromagnetic interference "EMI" difficulties, but using of suitable elements and optimum design parameters can highly reduce and eliminate the effects of these associated problems [1], [2], [3].

2- Basic topologies of step-down buck converter

The traditional circuit diagram of the asynchronous-buck converter "ASBC" is shown in fig "1". The simplest construction of this topology consists of switching field effect transistor "FET" with L-C filter and rectifier diode "D", C_{in} is an input capacitor filter used to control the ripple associated with input DC voltage source V_{in}, V_{out} is the DC voltage across the load resistance RL that needed to be regulate by controlling the ON-time duration of a PWM signal feeding at the gate of switch field effect transistor "S1" [4], [5].
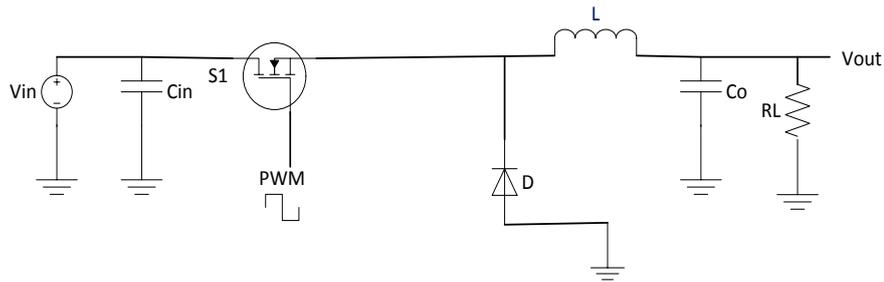
Fig (1) typical circuit diagram for asynchronous buck-convertor

In continuous conduction mode "CCM" in which the current passing through inductance " I_L " never fall to zero along hall time period of the PWM "T ", the average output dc-voltage is given by:

$$V_{out} = D \times V_{in}, \quad \text{" only when} \quad V_{in} > V_{out}\text{"} \qquad \ldots eq1$$

$$D = \frac{T_{on}}{T}, \quad \text{where } T = T_{on} + T_{off} \text{ "} \qquad \ldots eq2$$

Fig(2) shows the basic diagram of synchronous buck-converter topology "SBC", the only modification is the rectifier diode is replaced by additional switch FET "S2" witch triggered on with an out-off phase signal to the PWM to make the diode work "one-way conduction flow" [5], [6].
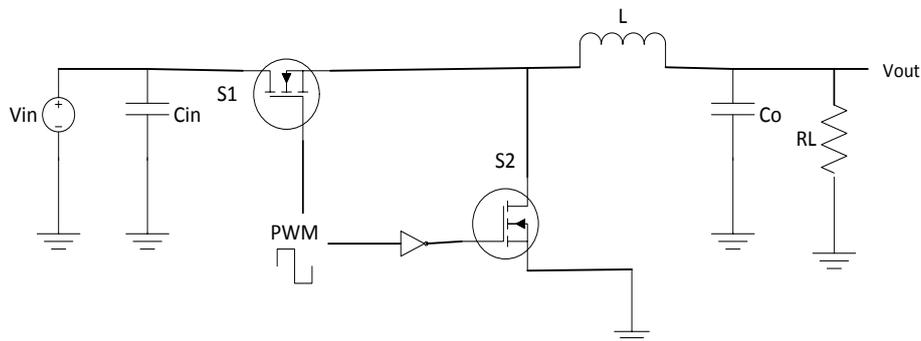
Fig (2) typical circuit diagram for synchronous buck-convertor

Usually synchronous buck-converter offers higher efficiency than asynchronous one, mainly due to the replacement of the diode by a FET switch, because the FET conduction resistance is small and does not have forward voltage drop across it like that with diode in the asynchronous topology.

The main disadvantage of the synchronous buck-converter is the higher cost compared with the asynchronous buck-converter, moreover the additional dead-space needed to separate the high-side FET "S1"and the low-side FET "S2" to prevent them from being energized at the same time, which may exceed the implementation size [6].

3- Methodology and the main goal of the work

In this paper both SBC and ASBC had been designed to satisfy CCM operation conditions and to supply a load current of "750mA" according to specific design considerations. Then the two designed topologies operated by using a range of switching frequency (150 KHz – 1 MHz) and three different values of duty cycle (0.4, 0.6, 0.8) respectively in order to study the effects of both switching frequency and duty cycle on the performance of the two topologies in term of efficiency.

4- Assumptions and considerations

Both topologies shown in fig (1) and fig (2) are assumed to work follows:

- DC input voltage "V_{in}" is (30 ± 4)V with ripple voltage "V_{inr}" of 250 mV
- output load current "I_{out}" is 750mA
- required output voltage "V_{out}" assumed to be 12V at the first test and then increased to 16 V, 24 V respectively with typical ripple index "V_r" less or equal to 1%
- From datasheet [7], MCH5809 composite N-channel MOSFET "MCH3443" with schottky barrier diode SBD SBS006M is suitable to use in both topologies according to suggested considerations in this work. This MOSFET offers low conduction resistance and ultrahigh-speed switching with short recovery time body diode.
- From data sheet [8] schottky diode "1N5820" offers low forward potential voltage "V_f" so that it can be used as rectifier diode in the ASBC topology.

Design of inductance "L"

Inductance value must keep current larger than zero in order to maintain system in CCM operation [5]. This condition mainly depends on the load resistance and minimum duty-cycle, the calculation of inductance is given in eqs3,

$$L_{min} = \frac{R_L(1 - D_{min})}{2F_{sw}} \qquad \text{... eq3}$$

$$R_L = \frac{V_{out}}{I_{out}} = \frac{12}{0.75} = 16 \qquad \text{... eq4}$$

$$D_{min} = \frac{V_{out}}{V_{in_{max}}} = \frac{12}{34} = 0.353 \qquad \text{... eq5}$$

In the same time minimum required inductance must be computed at minimum switching frequency "F_{sw}" used in this work (150 KHz) to ensure that the inductance value is suitable for the other higher switching frequencies used in this work.

$$L_{min} = \frac{16(1-0.353)}{2 \times 150000} = 29.5 \ \mu H \qquad \text{…eq6}$$

From inductors datasheet [9] an inductor of 79.38 µH/6A/0.04 Ω is suitable choice.

Design of output capacitance filter "C_{out}"

To select a suitable output capacitance filter, maximum allowable effective series resistance "rc_{max}" of the capacitor must be determined first. In fact, effective series resistance "ESR" of the capacitor is more important than the capacitance value itself because too large effective series resistance of output filter capacitance makes the voltage due to ripple current equalize or exceeds the target output ripple voltage "V_r" as seen in eq7 [5] ,

$$V_r = \Delta IL_{max} \times rc_{max} \qquad \text{... eq7}$$

Where "ΔIL_{max}" is the maximum inductor ripple current and it is given by:

$$\Delta IL_{max} = \frac{V_{out}(1-D_{min})}{L \times F_{sw}} = \frac{12V(1-0.353)}{79.38 \times 10^{-6}H \times 150000Hz} = 0.652A$$

In this work the target ripple index assumed to be equal or less than 1%, so that

$$V_r = 12 \times 0.01 = 0.12 \ V \quad \text{and}$$

$$rc_{max} = 0.12V \times 0.652A = 0.078 \ \Omega$$

Select "rc" to be 0.06 Ω, minimum output capacitance can be determined by eq8:

$$C_{out_{min}} = max \left\{ \frac{D_{max}}{2 \times F_{sw} \times r_c}, \frac{(1-D_{min})}{2 \times F_{sw} \times r_c} \right\} = \frac{(1-D_{min})}{2 \times F_{sw} \times r_c} = 36 \mu f \qquad \dots eq8$$

From capacitor datasheet [10], a capacitor of 330 µf/50V/0.06 Ω, is a suitable selection.

Design of input filter capacitor " C_{in}"

The most important factors that limits the value of the input capacitance is duty-cycle " D " and the ripple current at the DC input voltage as shown in eq9,

$$C_{in} = T_{on} / \left(\left(\frac{V_{inr}}{I_{inr}} \right) - rc_{in} \right) \qquad \dots eq9$$

The worst case of input ripple current in the step-down converter usually is 50% of the output load current [11], this case occurs when the duty-cycle is 50%, and input ripple current at such condition is shown in eq10:

$$I_{inr} = \frac{I_{out}}{2} = 0.375 \, A \qquad \dots 10$$

Assumed input ripple voltage V_{inr} in this work is 250 mv, if the selected effective series resistance "ESR"of the input filter capacitor " r_{cin} " was 125 mΩ, then "eq9" becomes as in eq11,

$$C_{in} = \frac{T_{on}}{0.542} \qquad \dots eq11$$

Where, $\quad T_{on} = \left(\frac{1}{f_{sw}} \right) - T_{off} \qquad \dots eq12$

Minimum switching frequency used in this work is 150 KHz, so that the ON-time at 50% duty-cycle "worst case" is 3.3µs, so that by applying eq11 the minimum required input capacitance is 6.15 µf.

From capacitor datasheet [10] a capacitor of 180 µf /50V/120 mΩ meet all needed requirements.

5- Sources of power losses and efficiency calculations

Buck-converters classified as high efficiency power supply, but still having many sources of power losses. Switching frequency and duty cycle effect on these sources in different degrees and manners, general equation of efficiency "ŋ" for both SBC and ASBC topologies is given by eq13:

$$\eta = \frac{P_{out}}{(P_{out} + P_{loss-t})} \qquad \dots eq13$$

"P_{out}" is the total output power,

$$P_{out} = V_{out} \times I_{out} \qquad \dots eq14$$

"P_{loss-t}" is the total power loss which is a combination of different sources of power losses in each topology [5], [6].

1. Power losses in synchronous buck converter topology

In this topology power losses is mainly due to losses generated in both high-side "S1" and low-side "S2" MOSFETs, moreover to losses due to inductance, input and output filter capacitors.

1.1 Conduction losses "P_{cond}" in high-side and low-side MOSFETs

It is generated by flowing drain current through the conduction resistance "R_{cond}" during ON-time duration T_{on} in high-side MOSFET and OFF-time in low-side MOSFET. Choosing small conduction resistance MOFET will be very helpful in the aim of reducing this type of losses [5], [12]. Conduction losses generated in high-side MOSFET " P_{cond-H}" is given by eq15:

$$P_{cond-H} = (I_{out})^2 \times R_{cond} \times D \qquad \dots eq15$$

According to assumption given in this work and the data-sheet of MC5809 MOSFET [7], conduction losses in high-side MOSFET can be given as in eq16:

$$P_{cond-H} = (0.75A)^2 \times 0.165\Omega \times D = 0.093D \text{ (watt)} \qquad \ldots eq16$$

At low-side MOSFET conduction losses can be given as in eq17 and eq18:

$$P_{cond-L} = (I_{out})^2 \times R_{cond} \times (1-D) \qquad \ldots eq17$$

$$P_{cond-L} = (0.75A)^2 \times 0.165\Omega \times (1-D) = 0.093(1-D) \text{ (watt)} \qquad \ldots eq18$$

1.2 Switching losses "P_{sw}"

It occurs during the transition interval of turning ON and OFF the high-side and low-side MOSFETs alternatively. It is highly depends on the rise time "t_{rise-L}" and fall time "t_{fall-L}" of the MOSFETs [5], [6], [13], [14], for high- side MOSFET switching losses "P_{sw-H}" can be calculated as in eqs (19-21):

$$P_{sw-H} = (\tfrac{1}{2}) \times V_{in} \times I_{out} \times (t_{rise-H} + t_{fall-H}) \times F_{sw} \qquad \ldots eq19$$

$$P_{sw-H} = \left(\tfrac{1}{2}\right) \times V_{in} \times 0.75A \times (20ns + 29ns) \times F_{sw} \qquad \ldots eq20$$

$$= 18.375 \times 10^{-9} \times V_{in} \times F_{sw} \text{ (W)} \qquad \ldots eq21$$

While in low-side MOSFET, switching losses can be depicted in eq22:

$$P_{sw-L} = \left(\tfrac{1}{2}\right) \times V_D \times I_{out} \times (t_{rise-L} + t_{fall-L}) \times f_{sw} \qquad \ldots eq22$$

Where "V_D" is the forward voltage for body diode in low-side MOSFET, for MC5809 MOSFET V_D is 0.47 V, and hence eq22 can be written as seen in eq23,

$$P_{sw-L} = \left(\tfrac{1}{2}\right) \times 0.47V \times 0.75A \times (20ns + 29ns) \times f_{sw}$$
$$= 8.6 \times 10^{-9} \times f_{sw} \qquad \text{(watt)} \qquad \ldots eq23$$

1.3 Reverse recovery losses "P_{rrbd}"

This type of losses is generated due to the transition of the body diode in low-side MOSFET when the high-side MOSFET go in to ON state. It is highly related to reverse recovery time of the body diode "t_{rrbd}" and the peak reverse recovery current of the body diode "I_{rrbd}" [12], [13]. This type of losses is increase with higher switching frequency and it is given by eq24:

$$P_{rrbd} = \frac{1}{2} \times V_{in} \times t_{rrbd} \times I_{rrbd} \times f_{sw} \qquad \ldots eq24$$

$$= \frac{1}{2} \times V_{in} \times 10 \times 10^{-9} \text{ (sec)} \times 200 \times 10^{-6} (A) \times f_{sw} \qquad \ldots eq25$$

$$= 10^{-12} \times V_{in} \times f_{sw} \qquad \text{(watt)} \qquad \ldots eq26$$

1.4 Internal output capacitance losses in the MOSFETs "$P_{oc-loss}$"

Output capacitance of the high side and low side MOSFET is charged during each switching cycle, which can produce losses and can be calculated totally for both high and low sides MOSFETs by eq27, [12],[13]:

$$P_{oc-loss} = \frac{1}{2} \times (C_{O-HS} + C_{O-LS}) \times V_{in}^2 \times f_{sw} \qquad \ldots eq27$$

Where C_{O-HS} and C_{O-LS} are the internal output capacitance of high and low side MOSFETs.

Using datasheet [7] eq27 can be written as follow:

$$P_{oc-loss} = \frac{1}{2} \times (22 \times 10^{-12} + 22 \times 10^{-12}) \text{ (F)} \times V_{in}^2 \times f_{sw} \text{ (Hz)}$$

$$= 22 \times 10^{-12} \times V_{in}^2 \times f_{sw} \qquad \text{(watt)} \qquad \ldots eq28$$

1.5 Gate charge losses "P_{Q-loss}"

This type of losses produce due to charging the gate in MOSFETs [12], [13], it can be totally calculated for both high and low sides MOSFETs by eq29:

$$P_{Q-loss} = (Q_{GS-H} + Q_{GS-L}) \times V_{GS} \times f_{sw} \qquad \qquad \ldots eq29$$

"V_{GS}" is the gate drive voltage for MOSFET " from data sheet [7] it is about 4(V), while Q_{GS} refered to equivalent gate to source charge in order to rise each MOSFET. For MOSFET "MC5809" Q_{GS} is about 0.52 nC, and gate-charge losses can be given by eq 30:

$$P_{Q-loss} = [0.52 \times 10^{-9}(C) + 0.52 \times 10^{-9}(C)] \times 4(V) \times f_{sw}(Hz)$$

$$= 4.16 \times 10^{-9} \times f_{sw} \qquad (watt) \qquad \qquad \ldots eq\ 30$$

1.6 Dead time losses "P_{d-loss}"

In synchronous buck converter if the MOSFETs "S1,S2" are turn ON simultaneously, a breakdown can be occurs by large short circuit current, In order to avoid such case it is very important to provide dead ON-time when the high-side switch"S1" is in ON-state while the low-side "S2" is in OFF-state and provide dead-OFF-time when the high-side switch is in OFF-state while low-side switch is ON-state. During those dead-times inductor current pass through body diode of the low-side MOSFET generating power losses, [6], [12], [13], [15].

In this paper a conventional fixed method was used to indicate the interval of the dead time. It is good approximation that to assume dead time for rising " t_{dr}" to be equal to twice the turn-on delay time of the used MOSFET, and assume dead time for falling " t_{df}" to be equal to twice of the turn-off delay time of the used MOSFET. Power loss due to dead-time can be calculated by:

$$P_{d-loss} = V_D \times I_{out} \times (t_{dr} + t_{df}) \times f_{sw}$$

From data sheet [7], for MOSFET "MC5809" turn-on delay time is 9 ns and turn-off delay time is 23 ns, so that dead-time losses can be given as in eq31,

$$P_{d-loss} = 0.47(V) \times 0.75(A) \times (2 \times 9 \times 10^{-9} + 2 \times 23 \times 10^{-9})sec \times f_{sw}(Hz)$$

$$P_{d-loss} = 22.56 \times 10^{-9} \times f_{sw} \qquad (watt) \qquad \qquad \ldots eq31$$

1.7 Inductance losses "P_{ESRL}"

DC losses generated when the current pass through winding of the inductor is increase as the length of the winding increase and decrease with increasing the cross section of the winding [5]. If the effective series resistance of the winding is ESRL then the inductance losses is shown in eq32,

$$P_{ESRL} = I_{out}^2 \times ESRL = 0.75^2 \times ESRL = 0.5625\ ESRL \ (watt) \qquad \qquad \ldots eq32$$

From inductance datasheet [9], effective series resistance of the selected inductor is 0.04 Ω, so that by applying eq32,

$$P_{ESRL} = 0.0225 \ (watt).$$

1.8 Losses due to input and output capacitance $P_{C_{in}}$, P_{Cout}

Losses in capacitors directly depends on the r.m.s value of the capacitor current and the effective series resistance of the capacitor [4], [5], [13], r.m.s current in the input capacitor is given by eq33,

$$Irms_{C_{in}} = I_{out} \times \frac{\sqrt{(V_{in}-V_{out}) \times V_{out}}}{V_{in}} \qquad (A) \qquad \qquad \ldots eq33$$

So that power dissipated in the input capacitor is seen in eq34,

$$P_{C_{in}} = (0.75 \times \frac{\sqrt{(V_{in} - V_{out}) \times V_{out}}}{V_{in}})^2 \times ESR_{cin} \qquad \qquad \ldots eq34$$

Where " ESR_{cin} " is effective series resistance of the selected input capacitor.

From capacitor datasheet [10], ESR_{cin} is 125 mΩ, then power losses due to input capacitor can be seen in eq35,

$$P_{Cin} = (0.75 \times \frac{\sqrt{(V_{in}-12)\times 12}}{V_{in}})^2 \times 0.125 \quad \text{(watt)} \qquad \dots eq35$$

The losses due to output capacitor can be depicted as in eq36,

$$P_{C_{out}} = \left(\frac{(V_{in}-V_{out})\times V_{out}}{2\sqrt{3}\times (F_{sw}\times L\times V_{in})}\right)^2 \times ESR_{Cout} \qquad \dots eq36$$

Where " ESR_{cout} " is effective series resistance of the selected output capacitor. From capacitor datasheet the effective series resistance of the output capacitor is 0.06 Ω, so losses due to output capacitor is seen in eq37,

$$P_{C_{out}} = \left(\frac{(V_{in}-12)\times 12}{2\sqrt{3}\times (F_{sw}\times 79.38\times 10^{-6}\times V_{in})}\right)^2 \times 0.06 \quad \text{(watt)} \qquad \dots eq37$$

Total losses generated in the given synchronous buck-converter"P_{T-SBC}"

From equations 16,18,21,23,26,28,30,31,32,35,37, total power losses in the given synchronous buck converter suggested in this work can be given by eq38:

$$P_{T-SBC} = 0.093D + 0.093(1-D) + 18.375\times 10^{-9}\times V_{in}\times F_{sw}$$

$$+8.6\times 10^{-9}\times f_{sw} + 10^{-12}\times V_{in}\times f_{sw} + 22\times 10^{-12}\times V_{in}^2\times f_{sw}$$

$$+4.16\times 10^{-9}\times f_{sw} \quad + 22.56\times 10^{-9}\times f_{sw}$$

$$+ 0.0225 + \left(0.75\times \frac{\sqrt{(V_{in}-12)\times 12}}{V_{in}}\right)^2 \times 0.125$$

$$+\left(\frac{(V_{in}-12)\times 12}{2\sqrt{3}\times (F_{sw}\times 79.38\times 10^{-6}\times V_{in})}\right)^2 \times 0.06 \quad \text{(watt)} \qquad \dots eq38$$

2. Power losses in asynchronous buck- converter topology

In ASBC topology the power loses can be into high-side MOSFET "S1", inductance, input and output capacitors, moreover losses generated due to rectifier diode. Power losses in ASBC can be classified mainly as followed:

2.1 Losses generated due to conduction in high-side MOSFET "P_{cond-H}"

The power losses generated due to conduction in high-side MOSFET can be shown in eq39,

$$P_{cond-H} = (I_{out})^2 \times R_{cond} \times D \qquad \dots eq39$$

According to assumptions given in this work and the data-sheet of MC5809 MOSFET, the above equation can be written as in eq40,

$$P_{cond-H} = (0.75A)^2 \times 0.165\Omega \times D = 0.093\times D \text{ (watt)} \qquad \dots eq40$$

2.2 Switching losses " P_{sw-H}" in high-side MOSFET

Such losses occurs during the transition interval of turning ON and OFF the high-side MOSFET only and it is given by eq42:

$$P_{sw-H} = \left(\frac{1}{2}\right)\times V_{in}\times I_{out}\times (t_{rise-H} + t_{fall-H})\times f_{sw} \qquad \dots eq41$$

$$P_{sw-H} = \left(\frac{1}{2}\right)\times V_{in}\times 0.75A\times (20ns + 29ns)\times f_{sw}$$

$= 18.375 \times 10^{-9} \times V_{in} \times f_{sw}$ (watt)   eq42

2.3 Losses due to internal output capacitance in the high–side MOSFET

The losses generated due to internal output capacitance in the high-side MOSFET can be shown in equations (43-45),

$P_{oc-loss} = \dfrac{1}{2} \times (C_{O-HS}) \times V_{in}^2 \times f_{sw}$ ... eq43

$P_{oc-loss} = \dfrac{1}{2} \times (22 \times 10^{-12}) \,(F) \times V_{in}^2 \times f_{sw} \,(Hz)$ ... eq44

$P_{oc-loss} = 11 \times 10^{-12} \times V_{in}^2 \times f_{sw}$ (watt)   ... eq45

2.4 Gate charge losses

It is produced due to charging the gate in the high-side MOSFET as in eq46,

$\mathbf{P_{Q-loss}} = (Q_{GS-H}) \times V_{GS} \times f_{sw}$ ... eq46

From data-sheet, gate charge losses can be written as in eq47

$P_{Q-loss} = [0.52 \times 10^{-9}(C)] \times 4(V) \times f_{sw}(Hz) = 2.08 \times 10^{-9} \times f_{sw}$ (watt)   ... eq 47

2.5 Inductance losses

The losses due to inductance can be written as seen in eq48,

$P_{ESRL} = I_{out}^2 \times ESRL = 0.75^2 \times 0.04 = 0.0225$ (watt)   … eq48

2.6 Losses due to input and output capacitance

Losses due to i/p and o/p capacitance can be expressed by eq49 and eq50,

$P_{Cin} = (0.75 \times \dfrac{\sqrt{(V_{in} - 12) \times 12}}{V_{in}})^2 \times 0.125$ (W)   ... eq49

$P_{C_{out}} = \left(\dfrac{(V_{in} - 12) \times 12}{2\sqrt{3} \times (F_{sw} \times 79.38 \times 10^{-6} \times V_{in})} \right)^2 \times 0.06$ (watt)   ... eq50

2.7 Losses in the rectifier diode

Losses generated from working the rectifier diode can be divided into:

2.7.1 Conduction losses " P_{d-on} ",

which generates due to current flow through diode while the high-side MOSFET is OFF, it highly depends on the forward voltage of the diode and the output current, and it is given by eq51:

$P_{d-on} = I_{out} \times V_{d-on} \times (1 - D)$ …eq51

From the data sheet of the diode 1N5820 [8], forward conduction voltage at conducting current of (0.75 A) is approximately (0.35 V), so that the power loss here can be given and depicted by eq52,

$P_{d-on} = 0.75 \times 0.35 \times (1 - D) = 0.263 \times (1 - D)$ (watt)   ... eq52

2.7.2 Reverse recovery losses "P_{d-rr}"

It can be determined in the same method used to calculate the reverse recovery losses in the body diode of low-side MOSFET in the SBC, but here the MOSFET is replaced by diode,

$P_{d\text{-}rr} = \dfrac{1}{2} \times V_{in} \times t_{d-rr} \times I_{d-rr} \times f_{sw}$ ... eq53

where " t_{d-rr} " is the reverse recovery time of the diode and I_{d-rr} is the peak recovery current of the diode. Back to data sheet of diode 1N5820, the reverse recovery losses is seen to be as in eq54,

$P_{d\text{-}rr} = \dfrac{1}{2} \times V_{in} \times 10 \times 10^{-9}(s) \times 2000 \times 10^{-6}(A) \times f_{sw}$ (Hz)

$$= 10^{-12} \times V_{in} \times f_{sw}(Hz) \quad (watt) \quad \dots eq54$$

2.7.3 Dead time loss $\;"P_{d-loss}"$

Here the dead-time losses can be written as seen in equations 55 and 56

$$P_{d-loss} = V_D \times I_{out} \times (t_{dr} + t_{df}) \times f_{sw} \qquad \dots eq55$$

$$= 0.35\ (V) \times 0.75\ (A) \times (2 \times 9 \times 10^{-9} + 2 \times 23 \times 10^{-9})\sec \times f_{sw}$$

$$= 16.8 \times 10^{-9} \times f_{sw}\ (Hz) \quad (watt) \qquad \dots eq\ 56$$

Total losses in the asynchronous topology $"P_{T-ASBC}"$

Using equations 40,42,45,47,48,49,50,52,54,56 the total power losses in asynchronous buck converter "ASBC" suggested in this work is given by eq57:

$$P_{T-ASBC} = (0.093 \times D) + (18.375 \times 10^{-9} \times V_{in} \times f_{sw}) + (11 \times 10^{-12} \times V_{in}^2 \times f_{sw}) + (2.08 \times 10^{-9} \times f_{sw})$$
$$+ (0.0225) + \left((0.75 \times \frac{\sqrt{(V_{in}-12) \times 12}}{V_{in}})^2 \times 0.125 \right)$$
$$+ \left(\left(\frac{(V_{in}-12) \times 12}{2\sqrt{3} \times (F_{sw} \times 79.38 \times 10^{-6} \times V_{in})} \right)^2 \times 0.06 \right) + \left(0.263 \times (1-D) \right)$$
$$+ (10^{-12} \times V_{in} \times f_{sw})$$
$$+ (16.8 \times 10^{-9} \times f_{sw}\ (Hz)) \quad (watt) \qquad \dots eq57$$

5- Test investigation and discussion

The designed synchronous and asynchronous buck-converter topologies in this paper had been operated by using of PWM signal with switching frequency range of (150 – 1000) KHz. Then by the use of the equations (38) and (57), efficiency of each topology had been tested by using three duty-cycle values (0.4, 0.6, 0.8) respectively to derive three different output load voltages (12V, 18V, 24V) respectively and keep output load current at 750mA in each test. MATLAP software is used to calculate results.

Results of tests are shown in fig (3), fig (4) and fig (5) respectively, these results turn out the major facts below:

1. Efficiency of both topologies "SBC and ASBC" was gained each time the used duty-cycle became larger. This behavior was mainly due to restricting three loss components in synchronous topology and three loss components in the asynchronous one. In both topologies the losses generated due to input and output capacitors tend to be smaller with larger duty-cycle. The third loss component in synchronous topology that was shrunk with larger duty-cycle was losses generated due to conducting through the low-side MOSFET "S2". This was mainly because OFF-time interval tends to be shorter with larger duty-cycle leading to reduce the time of conducting in the low- side MOSFET. The same reason led to reducing the losses generated due to conducting through the diode in the asynchronous topology which highly depends on the length of OFF-time interval.
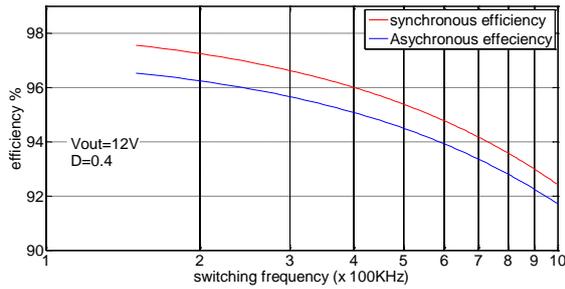
Fig (3) switching frequency vs efficiency of synchronous and asynchronous buck-converter at duty-cycle of 0.4
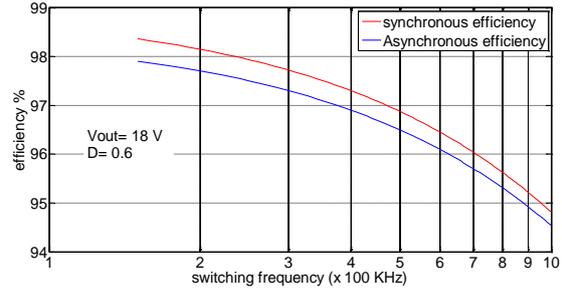
Fig (4) switching frequency vs efficiency of synchronous and asynchronous buck-converter at duty-cycle of 0.6
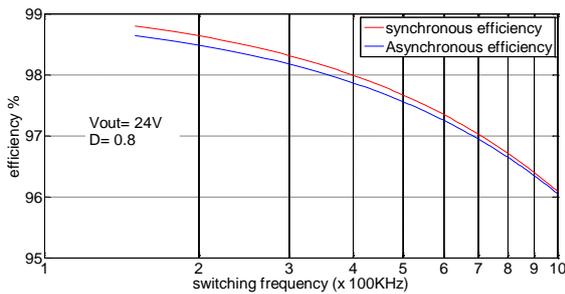
Fig (5) switching frequency vs efficiency of synchronous and asynchronous buck-converter at duty-cycle of 0.8
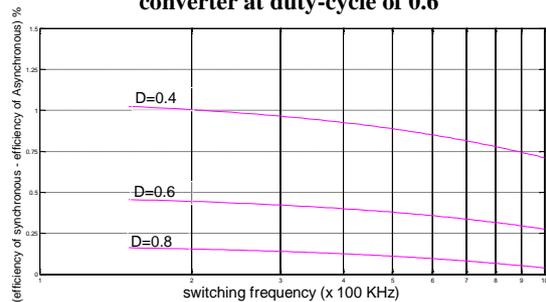
Fig (6) switching frequency vs deference in efficiency between synchronous and asynchronous buck-converter at duty-cycle of 0.4, 0.6, 0.8, respectively

In the same time it can be seen from the results that efficiency of both topologies became closer as the duty-cycle became larger, this influence is more clear in fig (6) in which the curve represents the difference in efficiency between SBC and ASBC topologies along the switching frequency range goes into lower level each time duty cycle was increased to larger value. This behavior came from the fact that losses generated due to conducting through diode during OFF-time represents the larger percentage of total loss power in ASBC topology compared with percentage losses generated due to conducting through low-side MOSFET in synchronous topology, so that losses due to conducting through diode in asynchronous topology was restricted in more severe manner than that in low-side MOSFET in synchronous topology when the duty-cycle goes higher.

Table (1) shows the recorded efficiency values of the two topologies at switching frequency of 1MHz according to duty-cycles used in the test investigation and output load current 750 mA.

Table (1)			
Switching frequency= 1MHz,		output load current= 750 mA	
operated Duty-cycle	regulated Output load voltage (V)	recorded Efficiency of synchronous buck-converter %	recorded Efficiency of asynchronous buck-converter %
0.4	12	92.5	91.6
0.6	18	94.9	94.5
0.8	24	96.2	96.15

2. The second fact that is concluded from the results given by figures (3,4,5) is that efficiency of both topologies tends to reduce when the used switching frequency became higher. This behavior resulted from existence many losses components depends on switching frequency in both

topologies, and these losses became larger with higher switching frequency. Effect of these components is not equal, and they increase with higher switching frequency in different amounts and manners, but in general the effect of these components became stronger with high switching frequencies and makes the losses that related to switching frequency represents the major factor of losses at certain band of frequencies.

Synchronous topology has three additional loss components affected by switching frequency than that in asynchronous one, these components related to low-side MOSFET, (switching losses, gate charge losses, losses generated due to internal capacitance). The additional loss components express the main reason of why the efficiency of synchronous topology reduce in a faster manner than the efficiency of the asynchronous topology when the switching frequency became higher. This influence become more clear at higher frequencies and leading to make efficiency of asynchronous topology to equalize the efficiency of synchronous topology at certain frequency and even become more efficient at higher frequencies especially when working at smaller output load currents and larger duty cycles.

6- Conclusions

Depending on results obtained in this work, increasing switching frequency leads to negative impact on efficiency level for both topologies synchronous and asynchronous buck converter but this negative impact is more severe on efficiency of synchronous topology. At smaller output load current the previous impact will amplify the weight of losses related to switching frequency compared to those related to conduction, and this impact made efficiency of both topologies to be very close even that performance of asynchronous topology become more efficient than that of synchronous topology in term of efficiency at a certain output load currents and switching frequencies.

It is good suggestion to work at larger duty cycle in the aim of magnifying efficiency of both topologies with such conditions of small load currents.

Previous conclusions suggest that if efficiency is on the top order in the design requirements, it is more efficient to use the asynchronous topology to deliver light loads especially with higher switching frequency and larger duty cycle. Additional advantages can be offered by the asynchronous topology like lowering cost and complexity of the design, and less EMI problems that occurs in synchronous topology at higher switching frequencies.

7- Suggested future work

In future, studying behavior of each loss component in both topologies separately with more focus in terms of switching frequency and duty-cycle will be very helpful in improving the performance and optimizing the design.

CONFLICT OF INTERESTS.

- There are no conflicts of interest.

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كفائة الدائرة الالكترونية النبضية لمخفض الجهد المستمر بنوعيه المتزامن والغير متزامن عند تشغيلهما لتجهيز تيار خرج صغير القيمة

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الخلاصة

في هذا البحث تم تصميم دائرة الكترونية نبضية لمخفض للجهد المستمر بنوعيه المتزامن والغير متزامن (SYNCHRONOUS AND ASYCHRONOUS BUCK-CONVERTER) للعمل في وضع توصيل مستمر (CCM).

لاحقا تم اختبار كفائة الدائرة النبضية لمخفض الجهد المستمر بهيكليه (المتزامن والغير متزامن) من حيث الكفائة عند تشغيلهما لتجهيز تيار خرج بقيمة صغيرة باستعمال نطاق قيم متعددة لنبضة الفتح المستعملة (SWITCHING FREQUENCY) يبداء من 150KHz الى 1MHz وكذلك بتطبيق ثلاثة اقيام منفصلة لزمن دورة التشغيل (DUTY-CYCLE) وهي 0.4 و0.6 و0.٨ على التوالي.

بينت النتائج المتحصلة في هذا البحث ان كفائة الدائرة الالكترونية لمخفض الجهد المستمر بهيكليه المتزامن والغير متزامن المصممة لتجهيز تيارات حمل قليلة تستجيب بشكل سلبي لزيادة قيمة تردد النبضة المفتاحية.

وعلى كل حال فعند العمل ضمن حدود تيارات خرج صغيرة فان الخسائر في القدرة الكهربائية ذات العلاقة بقيمة تردد النبضة المفتاحية (SWITCHING LOSSES) تتجه لان تكون أكبر من خسائر القدرة المتولدة جراء التوصيل (CONDUCTING LOSSES)، وهذا التاثير يؤدي الى جعل كفائة الدائرة النبضية لمخفض الجهد المستمر بنوعيه المتزامن والغير متزامن تتقارب في القيمة، خصوصا عند العمل باستخدام نبضات مفتاحية ذات ترددات اعلى. وبشكل عام فان زيادة قيمة زمن دورة التشغيل يؤدي الى رفع كفائة كلا النوعين المتزامن والغير متزامن.

الكلمات الدالة– الدوائر النبضية لمخفض الجهد المستمر، كفائة الدائرة النبضية لمخفض الجهد المستمر، منظم الجهد المستمر، وضع توصيل مستمر، زمن دورة التشغيل، خسائر القدرة الكهربائية ذات العلاقة بتردد الإشارة المفتاحية وبالتوصيل في الترانزستور ذو الشبكة المعزولة.