Fifth Generation (5G) New Radio (NR) Channel Codes Contenders Based on Field- Programmable Gate Arrays (FPGA): A Review Paper

Ahmed A. Hamad

Department of Electrical Engineering, College of Engineering, University of Babylon, Hilla, Iraq

ahmedbabel@gmail.com

Mohammed Khalid Ibrahim

Department of Electrical Engineering, College of Engineering, University of Babylon, Hilla, Iraq

Dr.mohammed.Khalid2019@gmail.com

Abdulrasul A. Al-hayder

Department of Electrical Engineering, College of Engineering, University of Babylon, Hilla, Iraq

Ajwadi.haydari@gmail.com

Sarah Alaa Tamkeen

Department of Electrical Engineering, College of Engineering, University of Babylon, Hilla, Iraq

saraalaatamkeen1992@gmail.com

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Abstract

The increased demands for quality, like high throughput, low-latency, wide coverage, energy consumption, cost and reliable connections in mobile services, multimedia and data transmission impose the use of advance technical requirements for the next fifth-generation (5G) new radio (NR). One of the most crucial parts in the physical layer of the new generation is the error correction coding technique. Three schemes, namely; Turbo, low density parity check (LDPC), and polar codes are potentially considered as the candidate codes for both data and control channels. The competition is evaluated in terms of error correction capability, computational complexity, and flexibility. The parallelism, flexibility and high processing speed of Field-Programmable Gate Array (FPGA) make it preferable in prototyping and implementation of different codes. This paper presents a survey on the current literatures that deals with FPGA-based decoder design associated with the previously mentioned channel codes.

Keywords: Fifth generation **(**5G**),** New radio (NR), LDPC, Turbo Code, Polar code, FPGA

1. Introduction

In wire or wireless communication systems, the received data are sometimes differing from the transmitted one. This is practically due to the errors that induced by the employed channel. Noise, fading and the intentional or unintentional interference are the major sources of errors. The communication errors that Influence the transmitted data symbols mostly are correctable by using the channel coding techniques at the receiverDifferent coding schemes have been introduced since the publishing of "Shannon's channel coding theorem" for the first time in 1948 [1].

The principal idea of channel coding is to increase the distance between transmitted symbols which make it hard to be contaminated and more reliable at the receiving end. receiving an almost errors free signal. This is mainly accomplished by mapping the data symbols in one-to-one correspondence to symbols (coded symbols) located at a large vector space. At the transmitting side, each time the encoder accepts a block of k data symbols and then an m redundant symbols intentionally added to it to produce codeword of length $n > k$ coded symbols. This new word is transmitted over the channel. At the receiving side, the decoder can utilize the added redundant symbols to detect and correct the communication errors within the original k data symbols. If the channel accidentally imposes a severe level of noise or interference, more redundant symbols are needed to account the expected increment of errors. Transmitting longer coded word implies low coding rate $R_c = k/n$ and hence low bandwidth efficiency. Therefore, practical code is the one that is able to successfully detect and correct errors at rate R_c as close as possible to the channel capacity that is imposed by Shannon limit [1].

For about six decades, many researchers have been looking for codes capable of approaching this limit. In their pioneer work in [2], the authors introduced a novel structure of two parallel concatenated convolutional encoders combined by one interleaver and they called it turbo code. This code present unprecedented results in terms of closeness to Shannon limit (within 0.7 dB) and it is adopted in 3G and 4G mobile broadband standards.

In his doctoral thesis [3] , Gallager was first introduced a new block code and called it LDPC which was not taken seriously for a long time. Finally, by mid-1990s, several authors [4] & [5] were rediscovered it again. Due to its remarkable error performance specially for large codeword length, LDPC is considered as the main core of channel coding for several IEEE standards such as wireless LAN (IEEE 802.11n) [6], WiMax (IEEE 802.16e) [7] and DVB-S2 [8].

The last inventions in the way of achieving channel capacity are polar codes. They were presented firstly by Arikan in 2009 [9]. They have attracted a great attention due to the following two characteristics: Firstly, their deterministic construction making the implementation of their codecs are very simple related to LDPC or turbo codes which are often depend partially on random construction. Secondly, they can achieve symmetric capacity of memoryless channel with no error floor as their length tends to infinity.

Previously mentioned codes are competing to reserve a place into the control and data channels within the new 5G NR standard. They all seem to have the same opportunity to win the race. The decision to use one of these codes must be based on a comprehensive examination to know that it meets the 5G requirements. This imposes the physical implementation of these codes. One of the easiest approaches to accomplish this task is the use of FPGA device. Adopting this way will shorten the time required for prototyping and processing. Because of the probabilistic nature to the Bit Error Rate (BER) performance test, it may take days on computer while on FPGA it can take hours [10]. This is mainly due to the ability of parallel processing that FPGA characterized by.

2. THE 5G REQUIREMENTS

The 5G NR must be able to deliver a huge number of varied services provided across a diverse set of devices with different performance and latency requirements. The new radio must provide communications for very high bandwidth transmissions like streaming video as well as low latency communications for remote control vehicle communications as well as low data rate low bandwidth communications for machine type communications. However, this imposes new requirements on channel encoding that can be summed up in the following points:

A. Throughput

The standardization bodies that concerned with 5G NR planned to support a peak data throughput R of 20Gbps which is much larger than the 1Gbps provided by 4G [11]. This advancement in data rate will improve the buffering capacity during favorable channel conditions. It is also improving the applications that utilize data streaming like video transmission. Due to the implication of channel coding in NR, throughput can be divided into encoded processing throughput and decoded processing throughput. The former term refers to the total number of codeword bits processed per second and the second quantify the number of information bits per second and is equal to the encoded throughput multiply the coding rate R_c [12]. For instance, one half coding rate the peak encoded throughput of 40 Gbps should be achieved. This high transmission throughput imposes extensive use of parallel processing. Assuming an average number of iterations of order $I = 8$ per decoding process and the codec processor runs on $C = 500$ MHz clock frequency, then a total of $R \cdot I/C = 320$ parallel processor work together to achieve the required decoding throughput. Alternatively, a decoding of multiple codewords at the same time using multiple slow processor or unrolling and pipelining of different block on the same decoder is a good candidate to achieve high data throughput. The parallel architecture of FPGA is favorable in the design of such parallel decoders to achieve the designed throughput or instantiation interval.

B. Latency

The 5G developers targeted the end-to-end 0.5 ms latency [12]. This much better than the 10 ms that achieved by 4G. The ultra-low latency will allow many real time applications to run without delay and provides a sense of satisfaction to users. In general, the main two strategies that adopted to achieve low processing latency at channel decoder are; first, design of fast decoders, which encompass multiple processors that run jointly on the same received word. The estimated latency when using this approach is given by dividing the average data length of K= 1000 bits by the 20 Gbps proposed decoded throughput which implies a 50 ns of latency which is much lower than the end-to-end latency. The second approach to achieve high processing speed is to use multiple of slow decoders works simultaneously on multiple of received blocks. In FPGA, the reduction in latency and instantiation interval (II) can be achieved by the implication of pipelining and unrolling of loops and partition of arrays and matrices. This usually at the expense of larger utilization of silicon area.

C. Capability of Error Correction and/or Detection

The 5G NR aimed to design an error correcting codes that are capable of losing no more than 1 block for every 100,000 transmitted block due to communication errors. This actually will reduce the requirement of Hybrid Automatic Repeat reQuest (HARQ) and hence reduce latency.

D. Flexibility

Due to the wide range of applications that 5G should serve, the error correcting code must be adaptive in rate and codeword length. Using different code length will avoid the padding of wasteful dummy symbols and hence band efficient utilization of a communication channel.

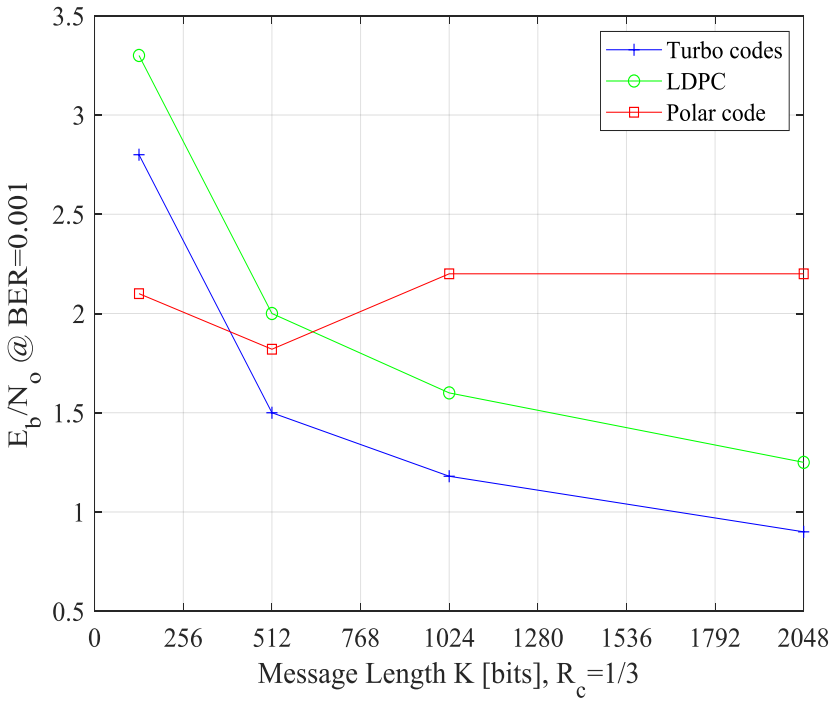
3. FPGA software aided design

There are several companies racing to produce different software platforms which provide a suitable environment to make implementation of different codecs. The two most famous companies in that field are Xilinx and Altera. Vivado and its older version ISE are presented by Xilinx whereas Altera produces Quartus and MAX+PLUS for market. These software programs are support different approaches to implement the designed circuit and generate a bit stream file to be downloaded in the FPGA device. For example, in Vivado, one can write its own HDL code (VHDL or Verilog) that describe the encoder and decoder circuit and convert it to RTL through synthesis, implementation and generate bit stream processes in sequence. Schematic is another way that using the available IP's in the Vivado repository or the exported ones from system generator or Vivado HLS. HLS supports high level of abstraction through the use of standard C/C++ or systemC. The synthesized RTL form HLS may export as an IP block either to Vivado or to system generator. Vivado also cooperate with MatLab through system generator environment which has Xilinx's block that can be mixed

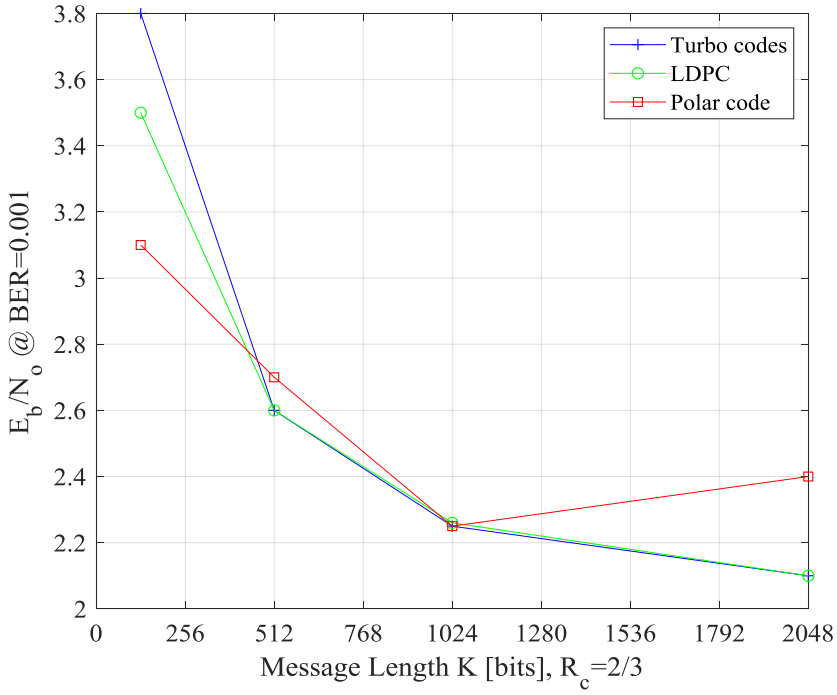
with native Simulink blocks to facilitate design and tests. System generator can produce hardware co-simulation JTAG or IP to accomplish the design.

4. Codes Comparison

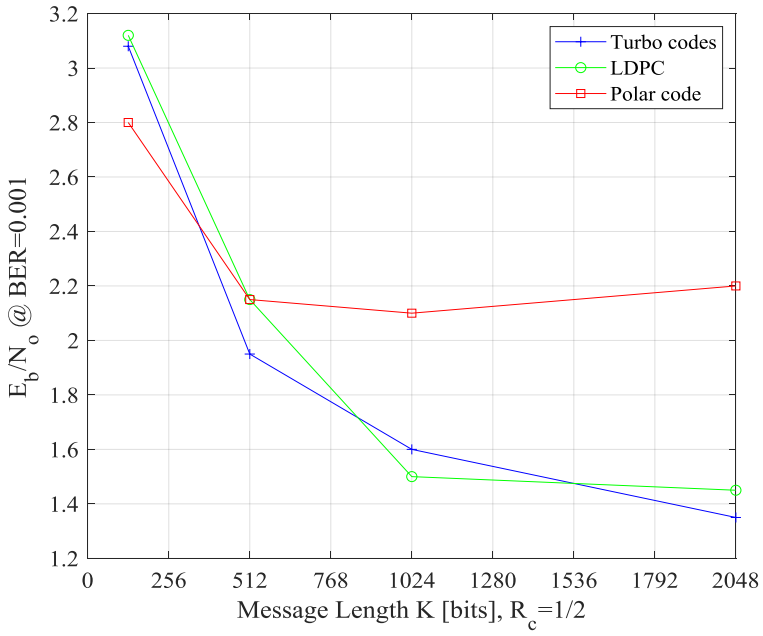
Applying QAM as modulation scheme, three of the nominated channel coding techniques are simulated over AWGN channel assuming perfect estimation of Channel state information (CSI). The first code is the LTE turbo code, with 4 constraint length and scaled MAX-Log-MAP decoder and 8 iterations. The second one is the LDPC code with channel code specifications presented in IEEE 802.11n. The Offset min-sum and 50 iterations is used at the decoder of LDPC simulations. The last one is the polar code with construction that based on the assumption of transmission over AWGN channel. At the receiver the (CRCA-SCL) decoder is employed in the simulation of polar code. A compression results are depicted in figures (1a-c) that show the required E_b/N_o to satisfy a Bit Error Rate (BER) of 0.003 at different coding schemes and different coding rate (R_c) and message length (K) [13]. We can remark the following observations: first, Polar code, in general outperform turbo and LDPC codes at low message lengths, but it gets worse at large lengths. Secondly, Turbo and LDPC codes have close performance for rates 1/2 and 2/3. Turbo code shows better behavior than LDPC at rate 1/3 over all values of K.



(a)



(b)



(c)

Figure (1): the required E_b/N_o to achieve BER=0.003 of coding schemes with different massage lengths and coding rate (R_c) equal to (a) 1/3, (b) 2/3 and (c) 1/2.

Figure (2) shows a comparison in complexity of the different coding schemes represented by the utilization area when implemented in application-specified integrated circuit (ASIC) [14]-[16]. The scatterplots show that the implementation of LDPC code is more efficient than turbo codes and polar codes.

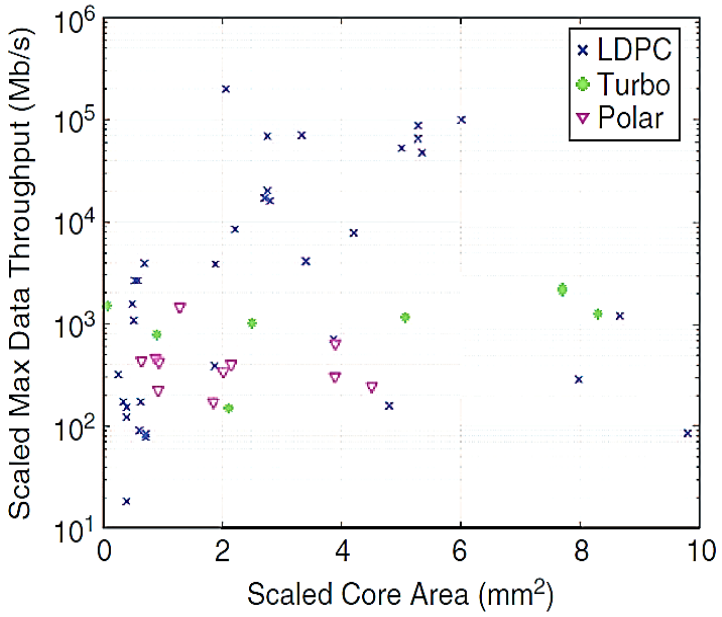


Figure (2): Scaled Chip area of ASIC required against scaled maximum achievable data throughput to implement LDPC, turbo and polar codes

Conclusion

This article provides an overview of the three codes; turbo code, LDPC and polar code which candidate channel coding schemes for the next 5G NR data and control signals. Turbo codes and LDPC almost have the same performance for different codeword length. On the other hand, polar codes exhibit better performance than the other coders for short block lengths (around 128 bits) with no error floor at high signal-to noise power ratio. Furthermore, the construction of polar codes is based on the proposed channel and hence it has the lack of versatility. The MAX-Log-MAP decoder of turbo codes and the minimum sum (MS) decoder of LDPC are more complex than the Successive Cancelation (SC) decoder of polar codes, yet its CRC aided SCL scheme exceeds the complexity of turbo and LDPC decoders. LDPC codes show relatively good performance in both area and energy efficiency.

Conflicts of Interest

The author declares that they have no conflicts of interest.

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مرمزات القناة المتنافسة على الجيل الخامس، الراديو الجديد، والمعتمدة على مصفوفات البوابات القابلة للبرمجة ميدانيًا: ورقة مراجعة

احمد عبد الكاظم حمد

قسم الهندسة الكهربائية، كلية الهندسة، جامعة بابل، الحلة، العراق

ahmedbabel@gmail.com

محمد خالد ابراهيم

قسم الهندسة الكهربائية، كلية الهندسة، جامعة بابل، الحلة، العراق

Dr.mohammed.Khalid2019@gmail.com

عبد الرسول عبد الحسين الحيدر

قسم الهندسة الكهربائية، كلية الهندسة، جامعة بابل، الحلة، العراق

Ajwadi.haydari@gmail.com

سارة علاء تمكين

قسم الهندسة الكهربائية، كلية الهندسة، جامعة بابل، الحلة، العراق

saraalaatamkeen1992@gmail.com

الخلاصة

ان الحاجة المتزايدة على الجودة، مثل السرعة العالية والتاخير المنخفض والتغطية الواسعة واستهلاك الطاقة والتكلفة والاتصالات الموثوقة في خدمات الهاتف المحمول والوسائط المتعددة ونقل البيانات تفرض استخدام المتطلبات التقنية المتقدمة في الجيل الخامس (5G) الإذاعة الجديدة (NR). واحدة من أهم الأجزاء في الطبقة المادية للجيل الجديد هي تقنية الترميز لتصحيح الأخطاء. هنالك ثلاثة اشكال مقترحة لتقنيات الترميز المخصصة لقنوات نقل البيانات وقنوات التحكم هي الترميز التوربيني وفحص التكافؤ المنخفض الكثافة (LDPC) والرموز القطبية. يتم تقييم المنافسة بين هذه الانواع من حيث القدرة على تصحيح الأخطاء والتعقيد الحسابي والمرونة. التوازي والمرونة وسرعة المعالجة العالية لمصفوفة البوابة القابلة للبرمجة الميدانية (FPGA) تجعلها أفضل في النماذج الأولية وتنفيذ الرموز المختلفة. تقدم هذه الورقة دراسة استقصائية للبحوث الحالية التي تتعامل مع تصميم وحدة فك الترميز المستندة إلى FPGA المرتبطة برموز القناة المذكورة سابقًا.

الكلمات الدالة: الجيل الخامس، الراديو الجديد، مرمز انخفاض كثافة التكافؤ، المرمز التوربيني، المرمز القطبي، مصفوفة البوابة القابلة للبرمجة الميدانية.